REMARKS/ARGUMENTS

Claims 1-21 are pending, and stand rejected under 35 U.S.C. § 102(e) as being anticipated by Blackmon et al. (US 2005/0021921 A1). New independent claim 21 has been added. No new matter has been introduced.

Applicants respectfully submit that independent claims 1, 12, 13, and 14 are novel and patentable over Blackmon et al. because, for instance, Blackmon et al. does not teach or suggest determining a processing sequence for the two or more information sets or the plurality of information elements, on the basis of the plurality of information elements that are unprocessed or currently being processed, contained in two or more information sets (or I/O requests) thus received, and determining a processing sequence different from a reception sequence, in which a value relating to the average of the response time for the two or more information sets (or I/O requests) becomes equal to or less than the value that would be obtained were the plurality of information elements or the two or more information sets (or I/O requests) to be processed in accordance with the reception sequence thereof.

The Examiner alleges that Blackmon et al. discloses the recited features at paragraphs [0022], [0025], [0028], and [0040].

Paragraph [0022] discloses a memory controller 140 that may couple with memory to re-order commands to access memory 160 based upon priorities and latencies associated with servicing the commands. There is no discussion of a value relating to the average of the length of processing time for two or more information sets or I/O requests.

Paragraph [0025] discloses a penalty box 142 that may track penalties of sequencers based upon latencies associated with servicing commands and communicate expirations of the penalties to a command queue 146. The penalty box 142 determines the latency in cycles, or penalty, associated with the store command and stores the penalty. There is no discussion of a value relating to the average of the length of processing time for two or more information sets or I/O requests.

Paragraph [0028] discloses a command queue 146 that may include one or more queues to store commands waiting for dispatch to an array controller 150. The command queue 146 may update penalties associated with commands that remain in the

queue in response to communication from the penalty box 142, dispatch commands to an available sequencer of the array controller 150, update each command associated with a sequencer to indicate the command is valid in response to input from the penalty box 142, select a command waiting in a queue when the next sequencer becomes available, and update the remaining commands associated with the same memory extent and bank as the selected command. There is no discussion of a value relating to the average of the length of processing time for two or more information sets or I/O requests.

Paragraph [0040] discloses a command queue 230 that may include load queue 232 and store queue 234 (for retaining commands in the order received to maintain a priority based on the order of receipt from processors), sequence tracker 236 (for maintaining associations between commands in the queues and associated sequencers to track penalties for the commands), prioritization logic 238 (for selecting between commands with expired penalties based on priorities associated with the commands and dispatching the commands as sequencers become available to receive the commands), fast path buffer 240 (for receiving commands of the highest priority), and interface monitor 242 (for monitoring dispatched commands and updating data in the sequence tracker 236). There is no discussion of a value relating to the average of the length of processing time for two or more information sets or I/O requests.

Blackmon et al. relates to re-ordering commands to access memory based on penalties associated with the commands. The penalties are calculated, tracked, and updated. The methodology is summarized in paragraph [0020]:

> Generally speaking, methods and systems for re-ordering commands to access memory are contemplated. Embodiments may receive a first command to access a memory bank of the memory and determine a penalty associated with the first command based upon a conflict with an access to the memory bank. The penalty, in many embodiments, may be calculated so the penalty expires when the memory bank and a data bus associated with the memory bank are available to process the first command. Then, the first command is queued and dispatched to an available sequencer after the penalty expires. Several embodiments select a command to dispatch from the commands with expired penalties based upon priorities associated with the commands such as the order in which the commands were received and the types of operations associated with the commands. After the first command is serviced, penalties of subsequent commands may be updated to reflect a conflict with servicing the first command (e.g., the first command

> may create new conflicts). Further embodiments, allow selected commands to bypass the queue when commands in the queue are waiting for their corresponding penalties to expire and no penalty is associated with the selected commands.

Significantly, there is no teaching or suggestion that the penalties are determined based on a value relating to the average of the length of processing time for two or more information sets or I/O requests, where a processing sequence is different from a reception sequence, in which the value becomes equal to or less than the value that would be obtained were the plurality of information elements or the two or more information sets or I/O requests to be processed in accordance with the reception sequence thereof. As discussed in the present application at page 5, lines 11-14, the present invention makes it possible to reduce the value relating to the average of the processing times taken to process a plurality of information sets.

For at least the foregoing reasons, claims 1, 12, 13, and 14, and claims 2-11 and 15-20 depending therefrom, are novel and patentable over Blackmon et al.

Applicants respectfully assert that new claim 21 is patentable over the cited references because, for instance, the references do not teach or suggest a determining component determining a processing sequence for the two or more I/O requests or the plurality of information elements, on the basis of the plurality of information elements that are unprocessed or currently being processed, contained in two or more I/O requests thus received, and determining a processing sequence different from a reception sequence, in which a value relating to the average of the response time for the two or more I/O requests becomes equal to or less than the value that would be obtained were the plurality of information elements or the two or more I/O requests to be processed according to the reception sequence thereof. Nor do they disclose a subsidiary expected value storing component storing subsidiary expected value information indicating subsidiary expected values relating to the length of time that processing is expected to take for information elements having certain information element attributes, for each of a plurality of information element attributes relating to the information elements; wherein the determining component acquires the subsidiary expected values for each of the plurality of information elements, on the basis of the respective information element attributes of the plurality of information

elements and the stored subsidiary expected value information, and acquires the expected values for each of the two or more information sets, by using the subsidiary expected values thus acquired; and a completion signal transmitting component transmitting a completion signal indicating that processing has been completed, to the information set source that issued an information set, when processing for the information set has been completed; wherein the length of processing time for the information set is a length of time relating to the response time from the issuing of the information set by the information set source until the reception of the completion signal by same.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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